Budapesti Műszaki és Gazdaságtudományi Egyetem

Közlekedésautomatikai Tanszék

Mechatronics and Microcomputers

Stipendium Hungaricum

2018/2019 Autumn Semester

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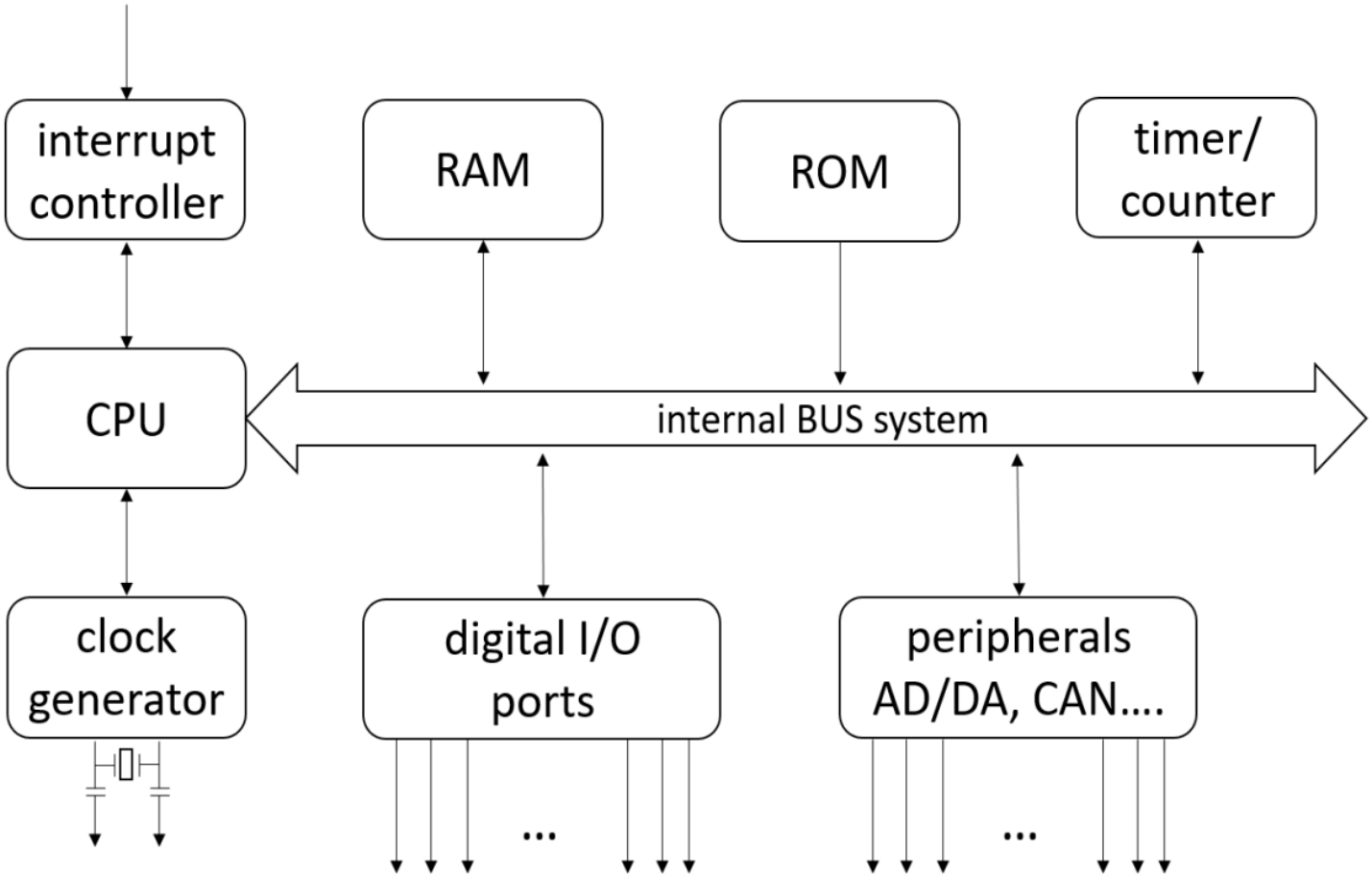
MCU architecture (repeat)



Definitions (MCU) I.

- CPU word size or bit width
  - word is a fixed-sized piece of data handled as a unit by the instruction set or the hardware of the processor. In embedded systems the processors usually have a word size of 8, 16, or 32 bits)
- ALU (arithmetic logic unit)
  - It is a fundamental part of the CPU, that performs arithmetic and bitwise operations on integer binary numbers.
  - Bitwise logical operations: AND, NOT, OR, XOR
  - Fixed-point arithmetic operations (two's complement integer): add, subtract, two's complement (negate), multiply, divide
  - Bit shift operations: shift, rotate

Definitions (MCU) II.

- Processor register
  - A quickly accessible location available to a CPU. A register usually consists of a small amount (1 or 2 words) of fast storage.
  - **Data register** can hold numeric data values such as integer characters or small bit arrays. In some older CPUs, a special data register, known as the accumulator, is used implicitly for many operations.
  - **Address registers** hold memory addresses and are used by instructions that indirectly access the memory. A special address register is the stack pointer which can be used to manage the stack.
  - **General-purpose registers** can store both data and addresses.
  - **Special-purpose or Special-function** registers hold program state; they usually include the program counter, also called the instruction pointer, and the status register. Microcontrollers can also have registers corresponding to specialized hardware elements.

Definitions (MCU) III.

- Input/Output port (IO, GPIO)
  - A multi-purpose digital signal pin on an integrated circuit or electronic circuit board whose behaviour—including whether it acts an input or output—is controllable by the user at run time. It provides an interface to other peripherals.
- Hardware Interrupt
  - An asynchronous signal to the processor emitted by a hardware peripheral indicating an event that needs immediate attention.
  - It alerts the CPU to a condition requiring interruption of the current code the processor is executing. The CPU responds by suspending its current activities, saving its state, and executing a function called an interrupt handler (or an interrupt service routine, ISR) to deal with the event. This interruption is temporary, and, after the interrupt handler finishes, the CPU resumes normal activities.

Definitions (MCU) IV.

- Timer/Counter
  - This peripheral simply counts with a register in sync with a pre-defined clock source. If the source is the microcontroller clock, we call it timer. If the source is an outer digital pulse, we call it timer.
  - Watchdog timer is special type of timers, which can realize safety function. It is used to detect and recover from computer malfunctions. During normal operation, the computer regularly resets the watchdog timer to prevent it from elapsing,. If, due to a hardware fault or program error, the computer fails to reset the watchdog, the timer will elapse and generate a timeout signal, which can initiate an action e.g. reset the processor.
  - Pulse-Width Modulation (PWM): a square wave signal with adjustable frequency and duty cycle.

Definitions (MCU) V.

- Universal Asynchronous Receiver/Transmitter (UART)
  - General purpose, two-wire, full- or half-duplex, asynchronous serial communication, in which the data format and transmission speeds are configurable. Basically it provides point-to-point connection with typically 115.2 kbit/s maximal speed. With the proper transceiver it can be used for RS-232, RS-422, RS-485, or LIN communication.
  - Another version is the USART, which is extended with a clock wire, thus it supports synchronous operation.
- Serial Peripheral Interface Bus (SPI)
  - A synchronous serial communication interface specification used for short distance communication, developed by Motorola. It is a four-wire serial bus using master-slave architecture. The master configures the clock, using a frequency supported by the slave device, typically up to a few MHz, but it is possible to find SPI adapters on the market today that support up to 100 MHz.
- Inter-Integrated Circuit (I^2C)
  - A synchronous, multi-master, multi-slave, serial computer bus invented by Philips Semiconductor.
  - The different specification releases supports different clock frequencies, typically 10, 100 and 400 kHz, but there exist releases with few MHz clocks.

Levels of Instructions

- In case of microcontroller programming three instruction levels exist
  - Programming language instruction (source code)
    - High-level
      - E.g. c=a+b;
    - Low-level (Assembly)
      - E.g. ADD R17,R16
  - Macro instruction
    - Compiled machine code
    - Built from the source code (compiler, linker, assembler)
  - Micro instruction (In case of microprogrammed CPUs)
    - Building blocks of macro instruction inside the CPU

Sturcture of Macro Instruction

- Operation code + memory address
  - Operation code (op code): operation
  - Memory address: operands
- 4 address operation
  - operand 1, operand 2, address of the result, address of the next operation
- 4 address operation
  - operand 1, operand 2, address of the result
- 2 address operation
  - operand 1, operand 2, result will be in one of the operands
- 1 address operation
  - operand 1, result will be in the operand

Downloading and Debugging

- Device programmer
  - In this case the MCU shall be put into an external device, which is conneted to the programmers PC via LPT, USB or LAN. After the manufacturing (soldering), the programming is not possible.
- In-system (In-circuit) Programming (ISP)
  - The program can be downloaded with USB programming device after the MCU is built (soldered) into the circuit. The debugging is not supported. Typically SPI is used for programming.
- In-circuit (Debugger) Emulator (ICE)
  - Same as the ISP, but it is possible to pause and follow the program step-by-step, watch the variables, registers and peripherals. This process is called debugging. Typical debugging communication technology is called JTAG.

MCU architectures I.

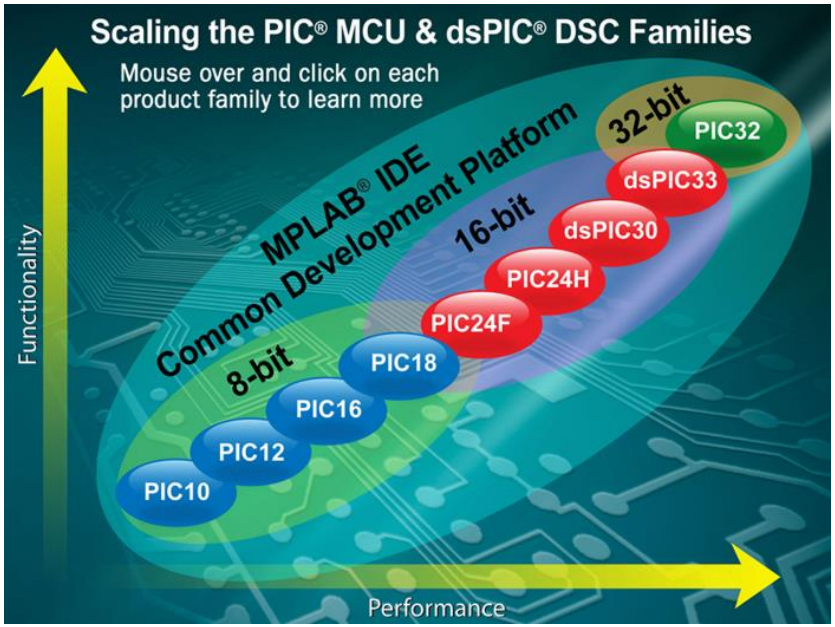
- MCS-51 (8051)
  - Developed by Intel in 1980
  - 8-bit, 128 byte RAM, 4 kbyte ROM, 4x8 I/O, UART
  - Very widespread
  - Intel stopped the manufacturing, but other IC manufacturers developed new version with extended memory and peripherals, but with the same instrucion set.
  - Some versions are used in automotive industry. (See e.g. Infineon XC800 family)

MCU architectures II.

- ARM (Acorn RISC Machine, Advanced RISC Machine)
  - The British computer manufacturer Acorn Computers first developed the Acorn RISC Machine architecture (ARM) in the 1980s to use in its personal computers. The official Acorn RISC Machine project started in October 1983.
  - In the late 1980s Apple Computer and VLSI Technology started working with Acorn on newer versions of the ARM core.
  - In 1990, Acorn spun off the design team into a new company named Advanced RISC Machines Ltd.
  - Today ARM Holdings' primary business is selling IP cores (reusable unit of integrated circuit), which licensees use to create microcontrollers (MCUs), CPUs, and systems-on-chips based on those cores.
  - Most widespread architecture mainly in consumer electronics
  - In 2013, 10 billion were produced[33] and "ARM-based chips are found in nearly 60 percent of the world's mobile devices„
  - Some examples from the manufacturers and devices built on ARM cores: Texas Instruments OMAP, Apple SoC, nVidia Tegra, Samsung Exynos, Qualcomm Snapdragon, MTK, Allwinner, Rockchip.
  - In automotive industry ARM is typically used in image processing.

MCU architectures III.

- PIC
  - Developed by Microchip Technology Inc. Very widespread microcontroller family.
  - From low-cost 8-bit devices to high-speed 32-bit DSPs
  - General purpose devices, but there exists automotive solutions as well.

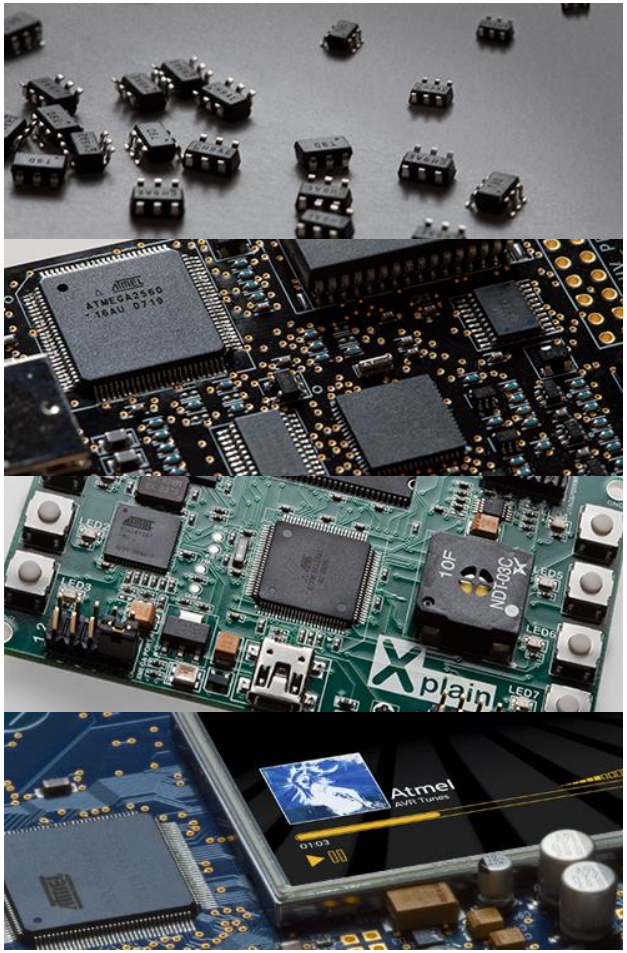


Atmel AVR architecture

- It is developed by two Norwegian university student in 1996. Later Atmel has bought the technology and the developers worked for Atmel.
- In 2016 Microchip acquired Atmel for 3.6 billion USD.
- Modified Harvard architecture, 8-bit, RISC
- The first MCU family, which uses flash memory for program storage (ROM).
- The pinout of the first 40-pins device (AT90S8515) was the same as the 8051 MCU.

Atmel AVR series

- tinyAVR (8-bit)
  - 0.5 – 8KB Flash, 6-32 pins
  - Max. 20MHz, 1.0 MIPS/MHz
- megaAVR (8-bit)
  - 4-256KB Flash, 28-100-pins
  - Max. 20 MHz, 1.0 MIPS/MHz
- AVR XMEGA (8/16-bit)
  - 16-384KB Flash, 44-100 pins
  - Max. 32 MHz, 1.0 MIPS/MHz
- 32-bit AVR
  - 16-512KB Flash, 48-144 pins
  - Max. 66 MHZ, 1.5 MIPS/MHz



Atmel megaAVR

- The most widespread Atmel AVR series.
- It contains about 100 different types
- Highly integrated devices (regarding to the memory and peripherals)
  - Integrated flash, SRAM, EEPROM
  - GPIO, SPI, TWI, USART, USB, CAN, LIN
  - Watchdog, internal and external clock sources
- Extensive analogue functions
  - A/D converter, built-in temperature sensor, internal voltage reference, brown-out detection, analogue comparator, programmable analogue amplifier

ATmega128 és AT90CAN128

- The only differences between the two types is the CAN communication
- RISC architecture
  - 133 instructions (most of them run in one clock-cycle)
  - 32 x 8 bit general purpose registers
  - Max. 16 MHz (1 MIPS/MHz)
- 128 Kb Flash, 4 Kb EEPROM, 4 Kb internal SRAM
- Peripherals
  - Two 8-bit and two 16-bit timer/counter
  - Two 8-bit and 6 programmable (2 – 16 bit) PWM channel
  - 8 channel, 10-bit A/D converter
  - 1 TWI (I2C), 2 USART, 1 SPI
  - Watchdog with own oscillator
  - Internal and external oscillator possibilities, six different sleep modes
- 64 pins TQFP package, 53 programmable I/O line

The End

Thank you for your attention!